

The block diagram illustrates the system architecture. It features several interconnected components:

- Input:** A signal labeled "17 DELAY" enters the system from the top left.
- FIT CHECKER (21):** Receives the "17 DELAY" signal and outputs to the STATE MACHINE (25).
- STATE MACHINE (25):** Receives input from the FIT CHECKER (21) and outputs to the ADDRESS GENERATOR (27) and the INDEX block (26).
- NUM_BIN (22):** Receives input from the FIT CHECKER (21) and outputs to the ROUTER (28).
- BIN_SIZE (23):** Receives input from the FIT CHECKER (21) and outputs to the ADDRESS GENERATOR (27).
- INDEX (26):** Receives input from the STATE MACHINE (25) and outputs to the ADDRESS GENERATOR (27).
- ROUTER (28):** Receives input from the NUM_BIN (22) block and outputs to the TSTORE[] ARRAY (15).
- ADDRESS GENERATOR (27):** Receives inputs from the STATE MACHINE (25), BIN_SIZE (23), and INDEX (26) blocks. It outputs to the BIN_ARRAY[] ARRAY (14).
- TSTORE[] ARRAY (15):** Receives input from the ROUTER (28) and outputs to the BIN_ARRAY[] ARRAY (14).
- BIN_ARRAY[] ARRAY (14):** Receives inputs from the ADDRESS GENERATOR (27) and the TSTORE[] ARRAY (15).

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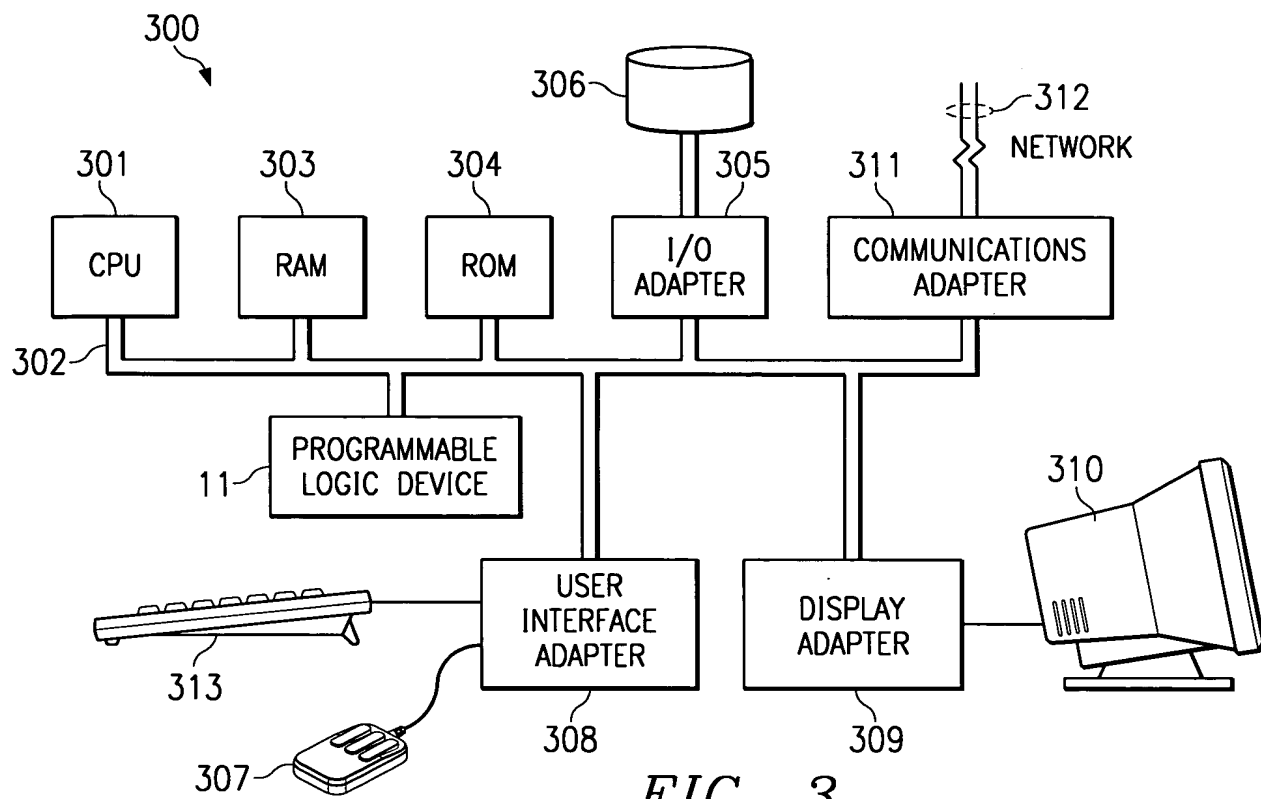


FIG. 3

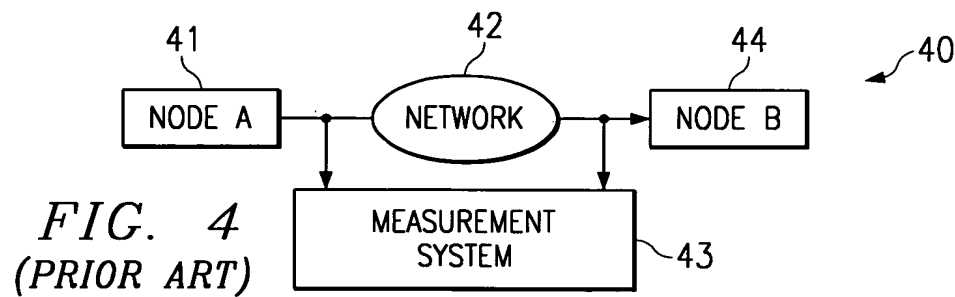


FIG. 4
(PRIOR ART)

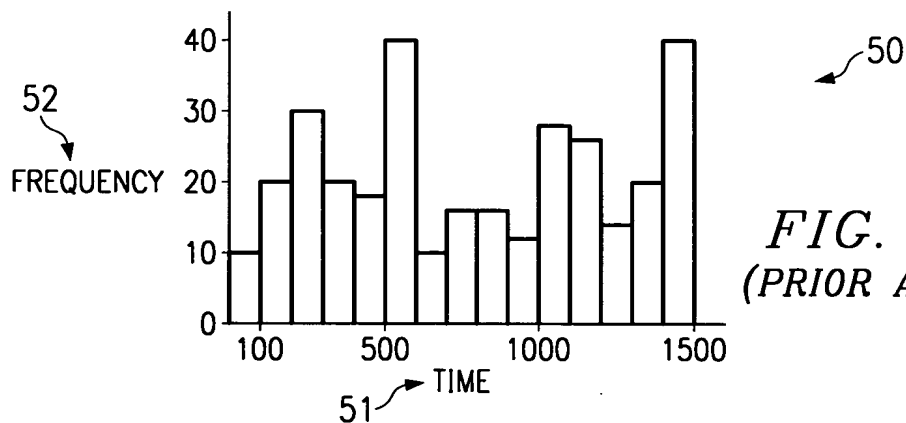


FIG. 5
(PRIOR ART)